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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,044	06/24/2003	Takekazu Tanaka	8053-1015	1342

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YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
CHAMBLISS, ALONZO	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,044	TANAKA, TAKEKAZU	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,23 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 1/25/06 has been considered and made of record in the application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-17, 23, and 24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 9 and 13 are objected to because of the following informalities: the word " encapsulation " is misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-10 and 25-28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Takahashi et al. (JP 2000-049184).

With respect to Claim 1, Takahashi at least one plate-like mount 3 and a semiconductor chip 7 having at least one electrode 11 formed on a top surface thereof.

The chip 7 is mounted on the plate like mount 3 such that a bottom surface is in contact with the plate-like mount 3. At least one lead element 5 having an outer portion that is substantially coplanar with the plate-like mount 3, and an inner portion deformed and shaped to overhang (i.e. above) the semiconductor chip 7 such that an inner end of the lead element 5 is spaced apart from the top surface of the semiconductor chip 7 without being mechanically connected to the chip 7. A bonding-wire element 14 is bonded at ends thereof to the electrode 11 of the semiconductor chip 7 and the inner end of the lead element 5. An enveloper 2 sealing and encapsulating a portion of the plate-like mount 3, the semiconductor chip 21, the inner portion of the lead element 5, and the bonding-wire element 14 (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claim 2, Takahashi teaches the electrode is defined as a first electrode and the lead element is defined as a first lead element. The semiconductor chip further having a second electrode 12 formed on the top surface thereof. The semiconductor package further comprising a second lead element having an outer portion arranged to be flush with the plate-like mount and an inner portion deformed and shaped to overhang the semiconductor chip such that an inner end of the second lead element is directly (i.e. via the bonding wire 14) and electrically connected to the second electrode 12 of the semiconductor chip (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claim 6, Takahashi teaches wherein the electrode is defined as a first electrode and the lead element is defined as a first lead element. The semiconductor chip further having a second electrode 12 formed on the top surface thereof. The semiconductor package further comprising a second lead element 6 having an outer portion arranged to be flush with the plate-like mount. The second lead element 6 has an inner portion deformed and shaped to overhang the semiconductor chip such that an inner end of the second lead element is spaced apart from the top surface of the semiconductor chip. At least one bonding-wire element 14 bonded at ends thereof to the electrode of the semiconductor chip and the inner end of the second lead element 6 (see paragraphs 54-58; Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claims 3, 7 and 10, Takahashi teaches wherein the chip is constructed as a MOSFET chip having a drain electrode 10 formed on a bottom surface thereof and electrically connected to the plate like mount, with the respective first and second electrodes being defined as a source electrode and a gate electrode, and the plate like mount has at least one lead element extending therefrom (see paragraphs 54-58; Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claims 4 and 8, Takahashi teaches wherein the MOSFET chip is formed as a high power type and the source electrode has a larger area than that of the gate electrode (see paragraphs 9, 10, 55, and 56; Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claims 5 and 9, Takahashi teaches wherein the sealing and encapsulation of the plate like mount in the enveloper is carried out such that a bottom surface to the plate like mount is exposed to outside (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claim 25, Takahashi teaches an island 3 (i.e. the portion of segment 3 does not have element 21). A MOSFET chip 7 mounted on the island and having a source electrode and a gate electrode formed on a top surface thereof. A first lead element 4 has an inner portion extending from the island. A second lead element 5 has an inner portion directly (i.e. via bonding wire) connected to the source electrode of the MOSFET chip 7. A third lead element 6 has an inner portion, which is spaced apart from the top surface of said MOSFET chip 7. A bonding-wire element 14 bonded at respective ends thereof to the gate electrode of the MOSFET chip 7 and the inner portion of the third lead element 6. An enveloper sealing 2 and encapsulating the island, the MOSFET chip 7, and the inner portions first, second and third lead elements 4, 5, and 6, and said bonding-wire element 14 (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claim 26, Takahashi teaches wherein outer portions of the first, second , and third lead elements project outward from the enveloper and are substantially coplanar with each other (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claim 27, Takahashi teaches wherein the island is connected to a drain electrode formed on a bottom surface of the MOSFET chip (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

With respect to Claim 28, Takahashi teaches wherein the enveloper is formed as a molded resin enveloper (see paragraph 54).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (JP 2000-049184) as applied to claims 1 and 10 above, and further in view of Crowley et al. (US 2003/0075785).

With respect to Claim 11, Takahashi discloses a semiconductor chip that is constructed as a diode chip see paragraph 8, which inherently has an anode and cathode electrodes. Takahashi fails to explicitly disclose chip having top and bottom electrodes being defined as an anode electrode and the remaining electrode being defined as a cathode electrode. However, it is well known in the semiconductor industry to have an anode electrode on one side and a cathode electrode on the remaining side of the diode as evident by Crowley (see paragraph 13). Therefore, it would have been obvious to one skilled in the art at the time of the invention to substitute a diode with an

anode and cathode electrode for the MOSFET of Takahahsi, since the diode would serve as a reliable high power semiconductor device for the semiconductor package as taught by Crowley.

With respect to Claim 12, Crowley discloses wherein the diode chip is formed as a high power type (see paragraphs 3 and 11-13).

With respect to Claim 13, Takahashi discloses wherein the sealing and encapsulation of the plate like mount in the enveloper is carried out such that a bottom surface of the plate like mount is exposed to outside (see Figs. 1-3, 10, 17, 18, 20-33, 39, 43, 46, 49, and 52).

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (JP 2000-049184) as applied to claim 1 above, and further in view of Nakamura et al. (US. 6,297,544).

With respect to Claim 23, Takahashi discloses the claimed invention except for an inner end of the lead element that is spaced apart from and directly overlying the top surface of a chip without being mechanically connected to the chip. However, Nakamura discloses an inner end of the lead element 2(2B) that is spaced apart from and directly overlying the top surface of a chip 3 without being mechanically connected to the chip 3 (see Fig. 3). Thus, Takahashi and Nakamura have substantially the same environment of a chip wire bonded to a lead wherein the chip and wire are encapsulated. Therefore, one skilled in the art at the time of the invention would readily recognize substituting a lead that is not mechanically connected to a chip for one of the leads of Takahashi, since the lead would provide a stable lead configuration for

electrical connecting an external device to a chip by wire bonding as taught by Nakamura.

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (JP 2000-049184) as applied to claims 1 and 25 above, and further in view of Uchida (US 2005/0121799).

With respect to Claim 29, Uchida fails to explicitly disclose wherein the first lead element is derived from a first lead frame and the second and third lead elements are derived from a second lead frame. However, Uchida discloses wherein the first lead element (i.e. external lead frame) is derived from a first lead frame and the second and third lead elements are derived from a second lead frame (i.e. inner lead frame) (see paragraphs 29-34). Thus, Takahashi and Uchida have substantially the same environment of a MOSFET wire bonded to a lead frame. Therefore, one skilled in the art would readily recognized incorporating 2 lead frames to form the first, second, and second lead elements of Takahahsi, since the 2 lead frames facilitate in the die mounting and wire bonding of the semiconductor die to the lead frames as taught by Uchida.

The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

9. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571)

272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

AC/March 31, 2006

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814